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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/276,803	03/26/1999	BYOUNG-TAEK LEE	SEC.506	2646

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EXAMINER
BEREZNY, NEAL

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/276,803	LEE ET AL.	
	Examiner	Art Unit	
	Neal Berezny	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 9 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Watanabe et al. (5,439,845). Watanabe teaches a method of building a capacitor comprising: forming a storage electrode over a semiconductor substrate, fig.2, el.28, forming a high dielectric layer over the storage electrode; fig.2, el.30, forming a plate electrode directly on the dielectric layer; el.32, performing a first anneal under an inert atmosphere at a first temperature; fig.1, el.94, col.15, ln.3-15, performing a second anneal, after the first anneal, at a second temperature lower than the first temperature in an oxygen environment; fig.1, el.96, col.15, ln.3-15, col.15, ln.32-35; the first and second anneals being performed after the forming of the plate electrode; fig.1, and wherein the plate electrode is formed of Pt; col.7, ln.32-38.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-5, 7-8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (5,439,845), further in view of Ping et al. (5,882,979). Watanabe et al. (5,439,845) also teaches a first anneal at a first temp. of 600-800^{0}C, col.15, ln.3-15, a second anneal at 100-600^{0}C, col.15, ln.1-15, the high dielectric consisting of STO, BST, and PZT dielectrics, col.9, ln.5-9, wherein the anneals are performed in an electric furnace, col.15, ln.13, and wherein both the first and second anneals can both be performed either before or after patterning, col.15, ln.3-15.

5. Watanabe appears not to specifically state that the two anneals be conducted in-situ. Ping teaches performing various processes in-situ, col.3, ln.4-5, fig.1 and 2, including an anneal step. It would be obvious to one of ordinary skill in the art at the time of the invention to combine Ping with Watanabe to perform the two anneal process steps in-situ in order to reduce the risk of contamination from the external environment. Further, official notice is given that it is well known and commonly practiced to employ clustering tools and in-situ processing to reduce processing time and exposure to the external environment, especially when the processing steps are very similar, requiring minimal variations between steps.

6. Claims 11-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Ping as applied to claims 1-2, 4-5, and 7-10 above, and further in view of Al-Shareef et al. (6,162,744) and Wolf, Vol.1, p.57, 183, and 388-389. Watanabe and Ping appear not to specifically state that the constructed capacitors and devices be connected together with an interconnect structure, thus neglecting to form an interdielectric layer, nor perform an anneal after the formation of the

interdielectric layer, nor performing a third anneal at a third temperature after the first two anneals, wherein the third temperature is less than either the first or second temperatures.

7. Al-Shareef teaches forming an interdielectric layer over the plate electrode of the capacitor, col.5, ln.29-30. Wolf teaches performing various interconnect thermal processes, after the formation of the interdielectric layer, p.57, table 4, section 3, which in terms of structure and function are also anneals. Wolf also teaches a first anneal at 900^{0}C, to form a silicide, p.388-389, and a second or third anneal at a lower temperature, 300-450^{0}C, in an oxygen atmosphere, p.183. It would be obvious to one of ordinary skill in the art to combine the teachings of Azuma and Wolf to the anticipated processes of Al-Shareef, i.e. to perform thermal anneals after forming the plate electrode, to further include anneals, i.e. thermal interconnect processes, which would need to, or likely, be performed after either the formation of the plate electrode or after the formation of the interdielectric. It would be obvious to one of ordinary skill in the art to anticipate the process of forming an interdielectric layer over the capacitor, and performing one, two, or three of the anneals, i.e. thermal interconnect processes, after the formation of the interdielectric, to complete the device and provide a flat, low resistance interconnect. One would be motivated to combine Al-Shareef and Wolf with Watanabe in order to reduce the post capacitor thermal budget and reduce the risk of oxidation of either of the electrodes from any out-diffusion of oxygen from the high dielectric layer, thereby reducing the capacitance of the capacitor. Official notice is given that it is well known in the art to form an interdielectric layer and that various

essential thermal interconnect processes, or anneals, are commonly performed throughout the industry, after the formation of the capacitor plate and the interdielectric layer. Further, such thermal processes, even when desired to be eliminated, cannot in practice be eliminated, because the consequences, for example, non-planarized topography or non-silicided interconnects would result in poorly functioning devices and severe processing problems in subsequent steps. In conclusion, it is an almost an unavoidable requirement of devices to undergo several anneals after the formation of the capacitor. It would be obvious to one of ordinary skill in the art to perform a third anneal at a lower temperature in order to reduce oxygen vacancy and densify the film. Further, it has been held that a mere duplication of a process step, or the division of a single step into multiple steps, involves only routine skill in the art. *St. Regis Paper Co.* v. *Bemis Co.*, 193 USPQ 8. In addition, neither the claims nor the specifications disclose the critical nature nor unexpected results arising from a third anneal.

Response to Arguments

8. Applicant's arguments with respect to claims 1-2, 4-5, 7-16, and 8-20 have been considered but are moot in view of the new ground(s) of rejection.

CONCLUSION

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neal Berezny whose telephone number is (703) 305-1481. The examiner can normally be reached on M-F 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NB
April 28, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800